VERSION HISTORY

K81Q1 Circuit diagram

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Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0	Release version	2020-03-12			

AllWinner Technology Co.,Ltd

Design Name: A100_B3_AXP707_LPDDR3

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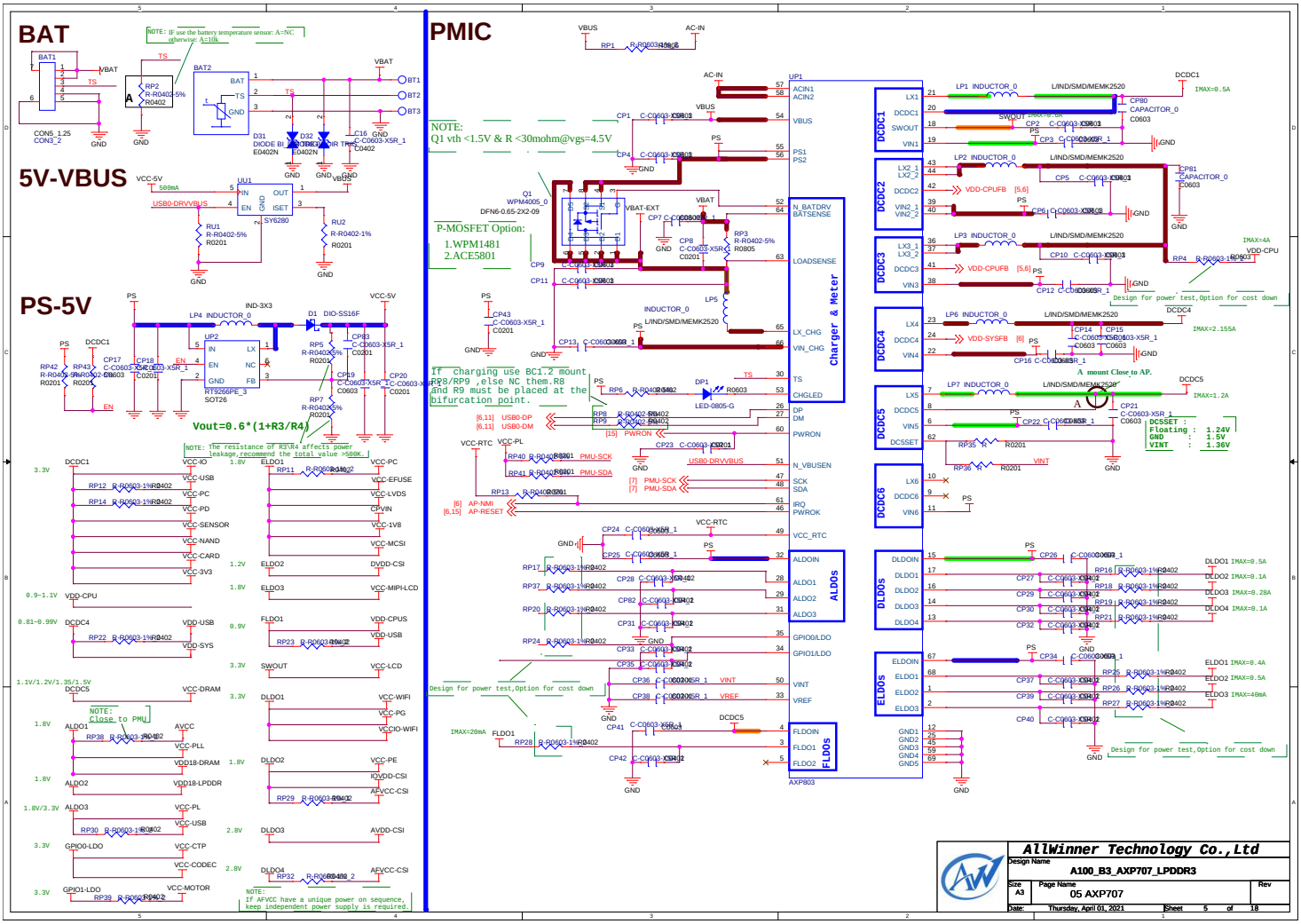
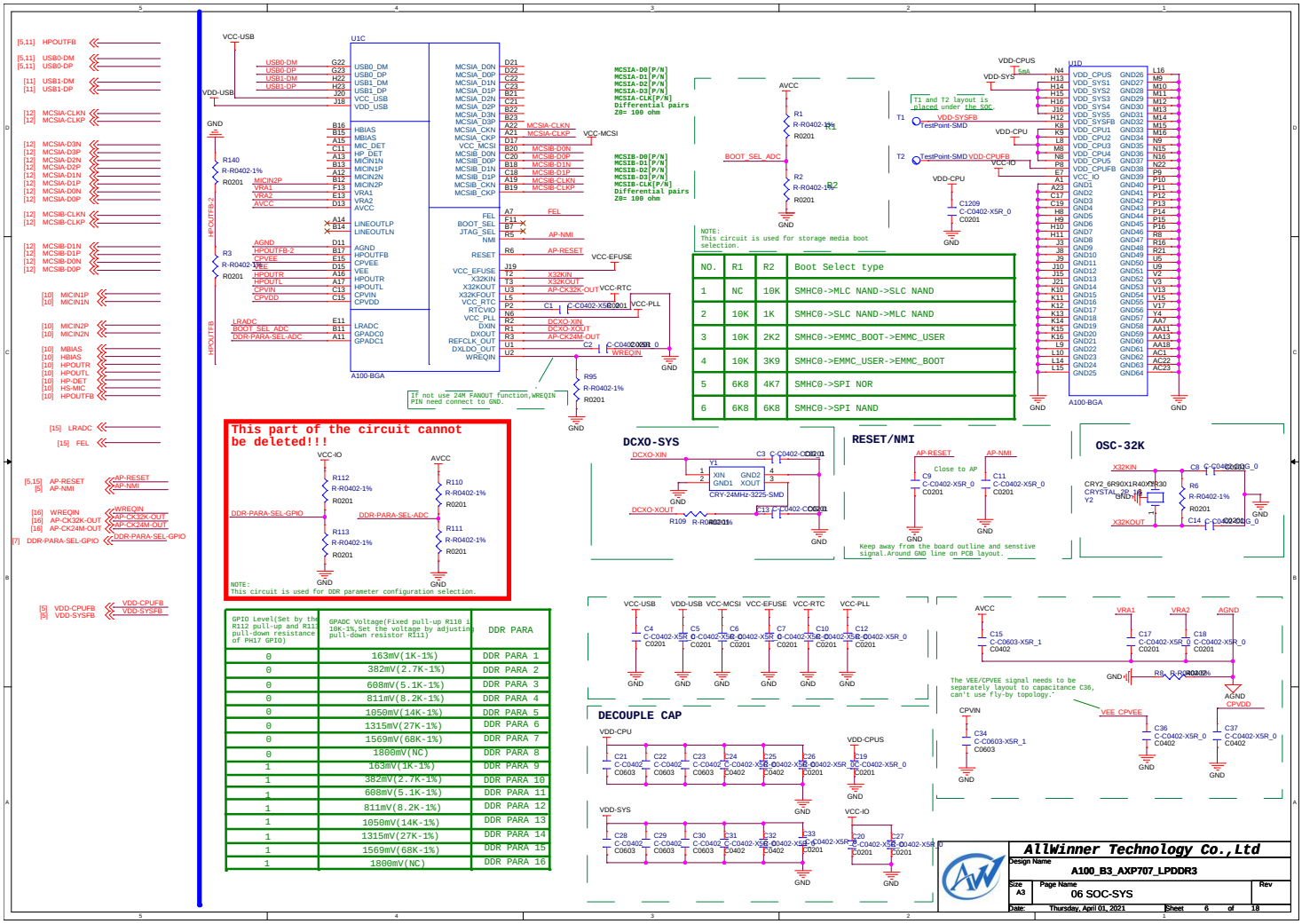

BAT
5V-VBUS
PS-5V
PMIC
Charger & Meter
ALDOs
DLDOs
ELDOs
FLDOs
DCDC1
DCDC2
DCDC3
DCDC4
DCDC5
DCDC6
AXP803
Vout=0.6*(1+R3/R4)
P-MOSFET Option:
1.WPM1481
2.ACE5801
AllWinner Technology Co.,Ltd
A100_B3_AXP707_LPDDR3
05 AXP707
Thursday, April 01, 2021



NO.	R1	R2	Boot Select type
1	NC	10K	SMHC0->MLC NAND->SLC NAND
2	10K	1K	SMHC0->SLC NAND->MLC NAND
3	10K	2K2	SMHC0->EMMC_BOOT->EMMC_USER
4	10K	3K9	SMHC0->EMMC_USER->EMMC_BOOT
5	6K8	4K7	SMHC0->SPI NOR
6	6K8	6K8	SMHC0->SPI NAND

GPIO Level(Set by the R112 pull-up and R113 pull-down resistance of PH17 GPIO)	GPADC Voltage(Fixed pull-up R110 is 10K-1%,Set the voltage by adjusting pull-down resistor R111)	DDR PARA
0	163mV(1K-1%)	DDR PARA 1
0	382mV(2.7K-1%)	DDR PARA 2
0	608mV(5.1K-1%)	DDR PARA 3
0	811mV(8.2K-1%)	DDR PARA 4
0	1050mV(14K-1%)	DDR PARA 5
0	1315mV(27K-1%)	DDR PARA 6
0	1569mV(68K-1%)	DDR PARA 7
0	1800mV(NC)	DDR PARA 8
1	163mV(1K-1%)	DDR PARA 9
1	382mV(2.7K-1%)	DDR PARA 10
1	608mV(5.1K-1%)	DDR PARA 11
1	811mV(8.2K-1%)	DDR PARA 12
1	1050mV(14K-1%)	DDR PARA 13
1	1315mV(27K-1%)	DDR PARA 14
1	1569mV(68K-1%)	DDR PARA 15
1	1800mV(NC)	DDR PARA 16

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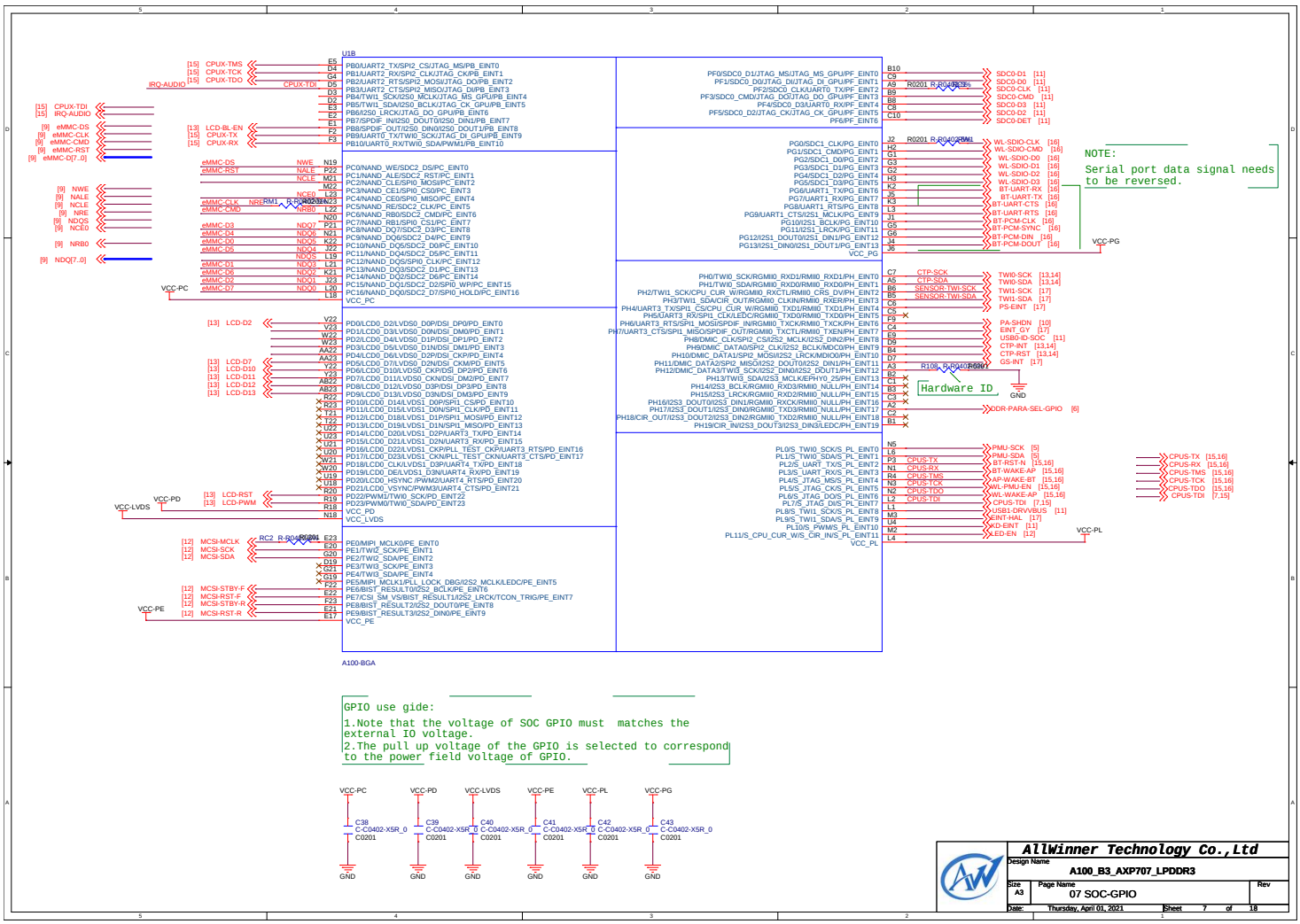
U1B
A100-BGA
NOTE:
Serial port data signal needs to be reversed.
Hardware ID
GPIO use gide:
1.Note that the voltage of SOC GPIO must matches the external IO voltage.
2.The pull up voltage of the GPIO is selected to correspond to the power field voltage of GPIO.
VCC-PC
VCC-PD
VCC-LVDS
VCC-PE
VCC-PL
VCC-PG
C38 C-C0402-X5R_0 C0201
C39 C-C0402-X5R_0 C0201
C40 C-C0402-X5R_0 C0201
C41 C-C0402-X5R_0 C0201
C42 C-C0402-X5R_0 C0201
C43 C-C0402-X5R_0 C0201
GND
AllWinner Technology Co.,Ltd
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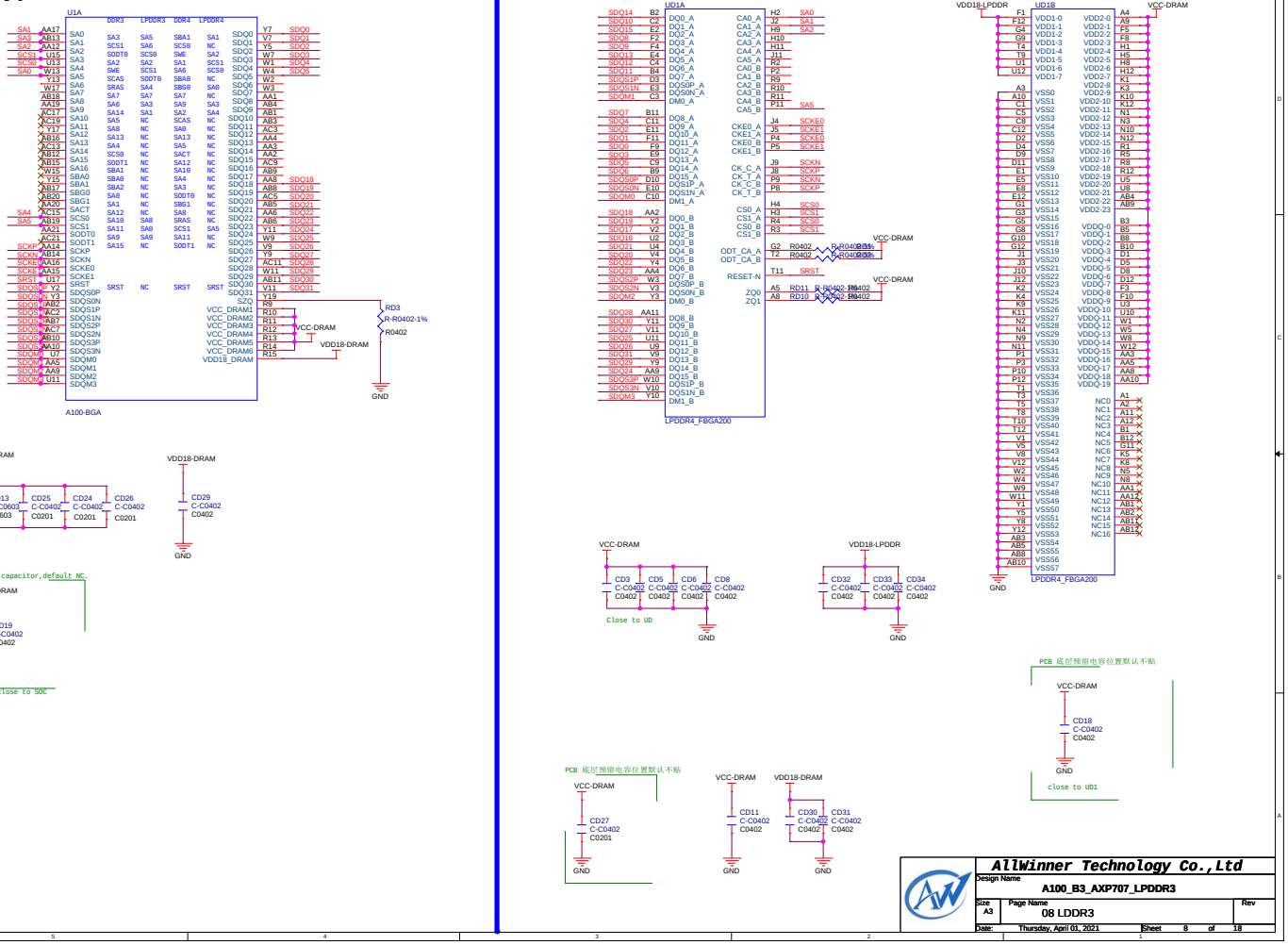
LPDDR4



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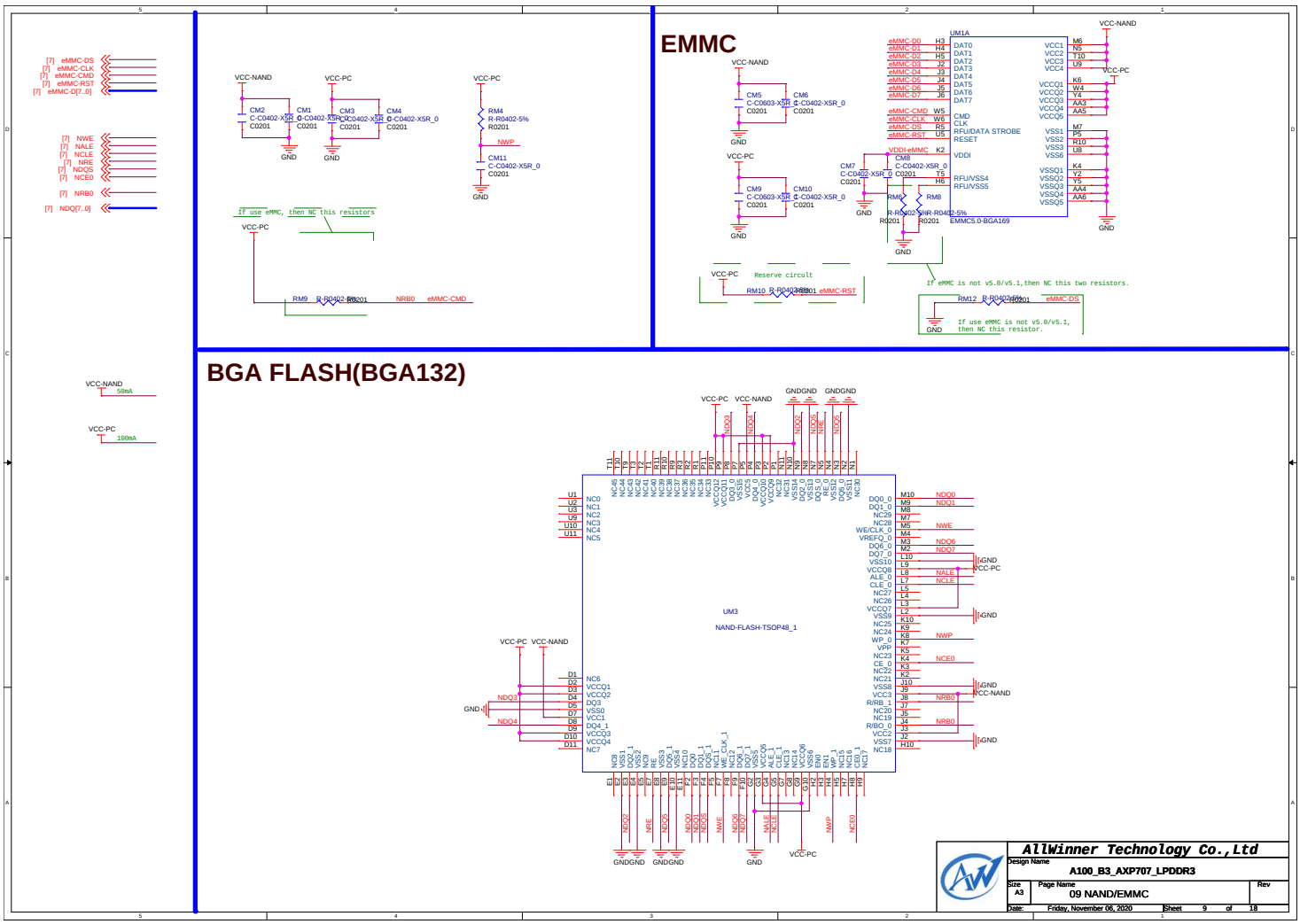
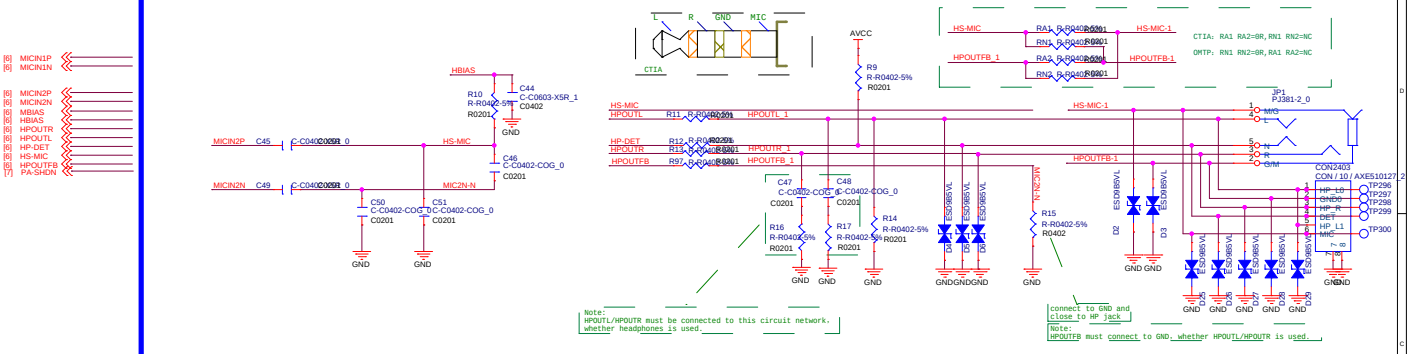
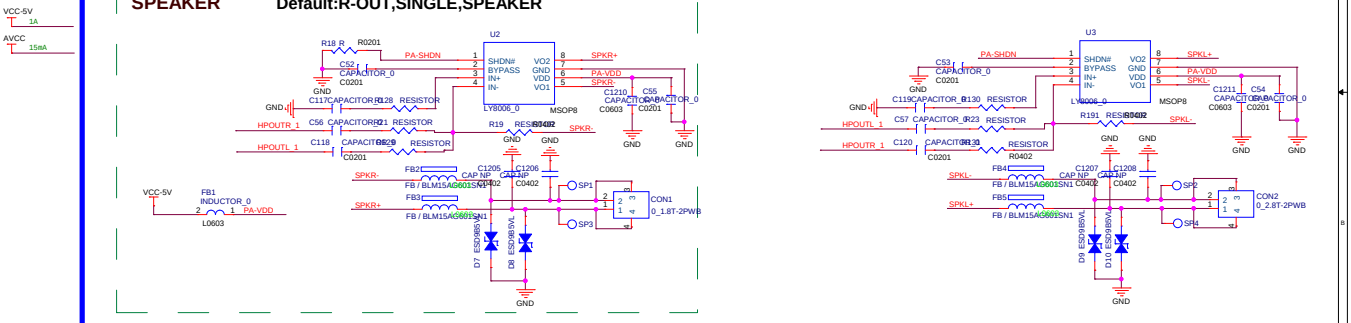

EMMC
BGA FLASH(BGA132)
UM1A
UM3
NAND-FLASH-TSOP48_1
EMMC5.0-BGA169
VCC-NAND
VCC-PC
GND
Reserve circuit
If use eMMC, then NC this resistors
If eMMC is not v5.0/v5.1,then NC this two resistors.
If use eMMC is not v5.0/v5.1, then NC this resistor.
AllWinner Technology Co.,Ltd
A100_B3_AXP707_LPDDR3
09 NAND/EMMC
Friday, November 06, 2020

HEADPHONE

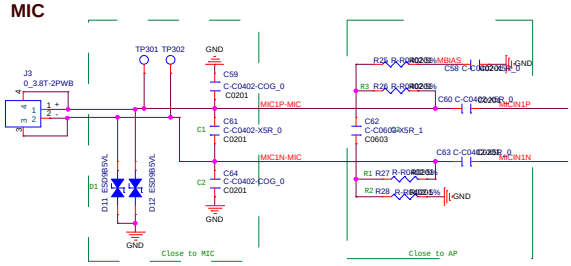


SPEAKER

Default:R-OUT,SINGLE,SPEAKER



MIC



Component	Diferential	single-ended
R1 R2 C1 C3 D1	USE	NC
C2	33pF	0R
R3	1.5K	1K

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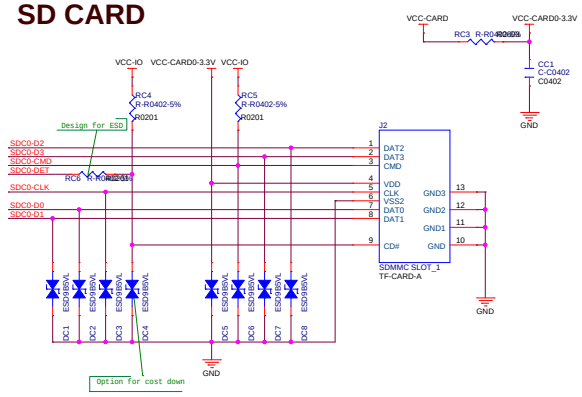
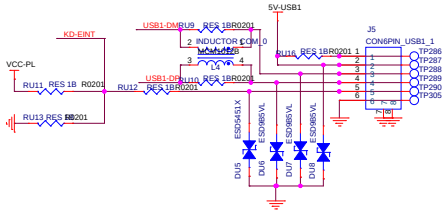
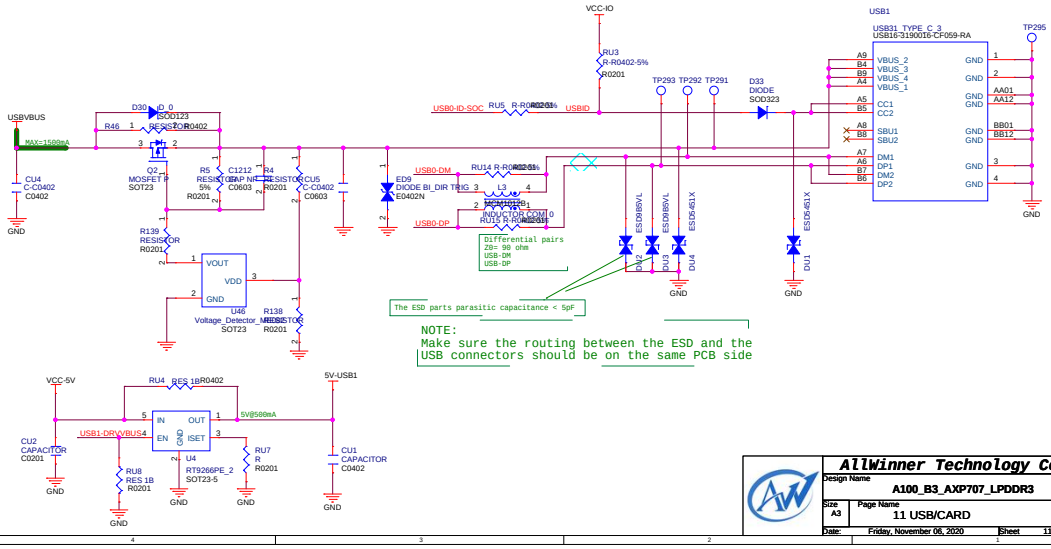
SD CARD



POGO



USB



[7] SDC0-D1
[7] SDC0-D0
[7] SDC0-CLK
[7] SDC0-CMD
[7] SDC0-D3
[7] SDC0-D2
[7] SDC0-DET

VCC-CARD — IMAX=0.8A
VCC-IO — 1mA

[5,6] USB0-DM
[5,6] USB0-DP
[6] USB1-DM
[6] USB1-DP

[7] KD-EINT
[7] USB0-ID-SOC
[7] USB1-DRVVBUS

VBUS
VCC-5V
VCC-PL — 10mA
VCC-IO — 1mA
VBUS — USBVBUS — 2A

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MCSIA-D0[P/N]
MCSIA-D1[P/N]
MCSIA-D2[P/N]
MCSIA-D3[P/N]
MCSIA-CLK[P/N]
Differential pairs
Z0= 100 ohm

MCSIB-D0[P/N]
MCSIB-D1[P/N]
MCSIB-CLK[P/N]
Differential pairs
Z0= 100 ohm

NOTE:
Because GC2385 and GC5025 has the same I2C address,
GC2385 and GC5025 cannot be used at the same time.

[6] MCSIA-CLKN
[6] MCSIA-CLKP
[6] MCSIA-D3N
[6] MCSIA-D3P
[6] MCSIA-D2N
[6] MCSIA-D2P
[6] MCSIA-D1N
[6] MCSIA-D1P
[6] MCSIA-D0N
[6] MCSIA-D0P

[6] MCSIB-CLKN
[6] MCSIB-CLKP
[6] MCSIB-D0N
[6] MCSIB-D0P
[6] MCSIB-D1N
[6] MCSIB-D1P

[7] MCSI-MCLK
[7] MCSI-SCK
[7] MCSI-SDA

[7] MCSI-STBY-F
[7] MCSI-RST-F
[7] MCSI-STBY-R
[7] MCSI-RST-R

[7] LED-EN

VCC-PE
R29 R-R0402-R0201 MCSI-RST-F
R30 R-R0402-R0201 MCSI-STBY-F
VCC-PE
R94 R-R0402-R0201 MCSI-RST-R
R31 R-R0402-R0201 MCSI-STBY-R

AFVCC-CSI AVDD-CSI IOVDD-CSI DVDD-CSI
C103 C-C0402 C0201
C66 C-C0402 C0402
C67 C-C0402 C0201
C68 C-C0402 C0201
GND GND GND GND

NOTE:
Close to connector
C65 C-C0402 C0201
GND
FLASH_VCC
R125 R-R0402-R0201
R124 R-R0402-R0201
R126 R-R0402-R0201

CON3
GND0 MDN3_B MDP3_B GND1 MDN2_B MDP2_B GND2 MDN1_B MDP1_B GND3 MDN0_B MDP0_B GND4 MCN_B MCP_B GND5 MDN1_F MDP1_F GND6 MDN0_F MDP0_F GND7 MCN_F MCP_F GND8 MCLK_F GND9 MCLK_B GND10 PWDN_F RESET_F RESET_B PWDN_B SCL SDA AF_VDD28 DVDD AVDD28 DOVDD18 40 41
CON39PIN_0
TP255 TP256 TP257 TP258 TP259 TP260 TP261 TP262 TP263 TP264 TP265 TP266 TP267 TP268 TP269 TP270 TP271 TP272 TP273 TP275 TP276 TP277 TP278 TP279 TP280 TP281 TP282 TP283 TP284 TP285

NOTE:
1.The working voltage and current of power need determine according to the peripheral specification.
2.AFVCC-CSI has timing requirements, don't share the same power with DOVDD-CSI.
3.The front and rear cameras need to consider the compatibility of DVDD-CSI voltage.

VCC-PE
R32 R-R0402-R0201 MCSI-SDA
R33 R-R0402-R0201 MCSI-SCK

VBAT 100mA
VCC-PL 10mA
AVDD-CSI 2.8V@30mA
IOVDD-CSI 1.8V@20mA
DVDD-CSI 1.2V@25mA
VCC-PE 10mA
AFVCC-CSI 2.8V@100mA

FLASH_LED

VCC-PL
FR1 R R0603
FC1 C-C0402 C0201
GND
VCC-PL
FR2 RES 1R R0201
FQ1 MOSFET N SOT23
FR4 R R0201
FC2 C-C0402 C0201
LED-EN
GND GND
FLASH_VCC
TP308
TP309
J6 PAD2PIN

AllWinner Technology Co.,Ltd			
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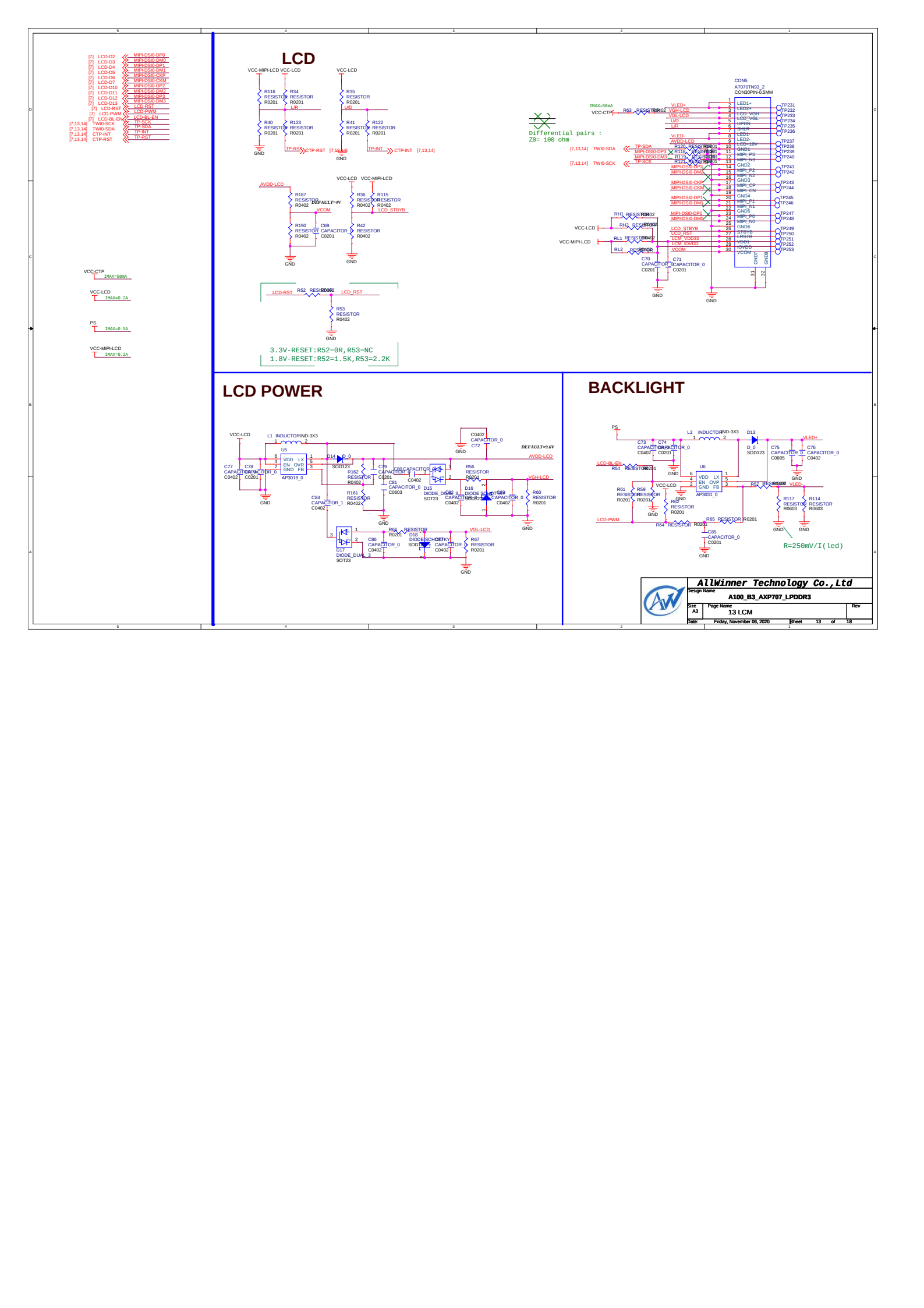
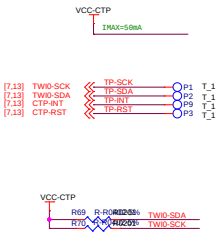
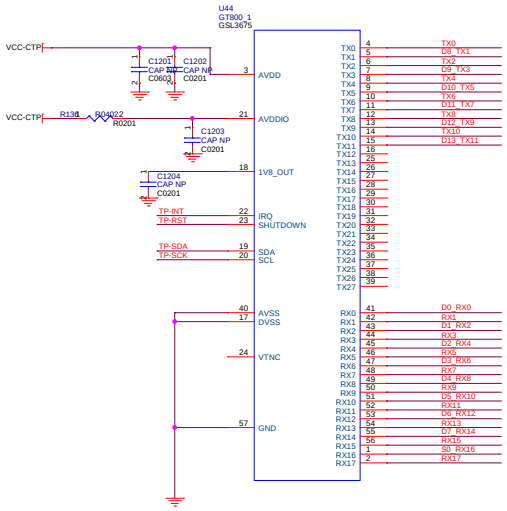
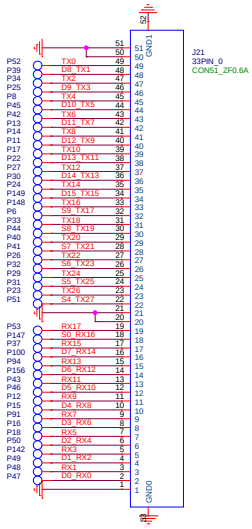

LCD
LCD POWER
BACKLIGHT
Differential pairs :
Z0= 100 ohm
3.3V-RESET:R52=0R,R53=NC
1.8V-RESET:R52=1.5K,R53=2.2K
R=250mV/I(led)
AllWinner Technology Co.,Ltd
A100_B3_AXP707_LPDDR3
13 LCM
Friday, November 06, 2020

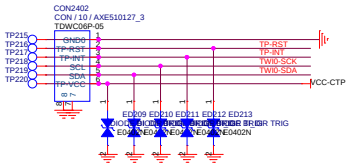
CTP

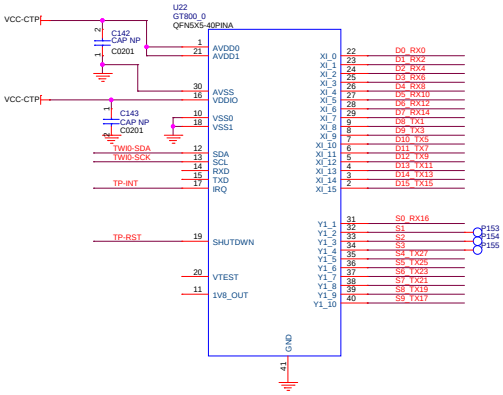


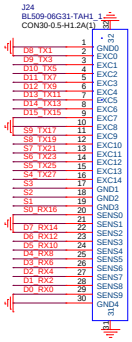




COF







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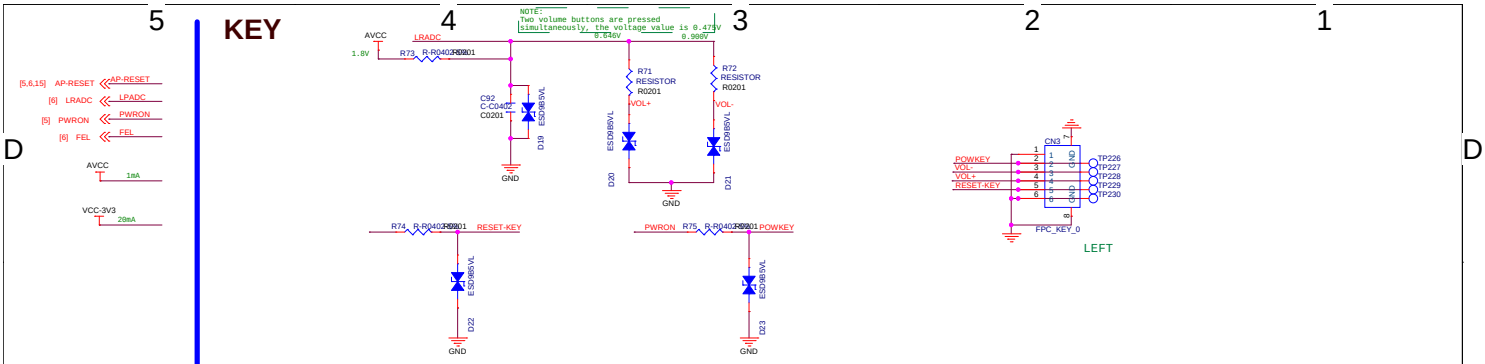
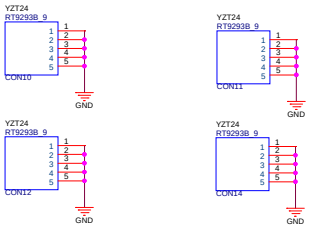
KEY

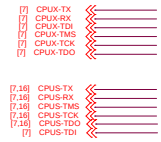


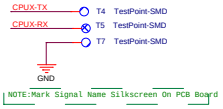
SHIELD

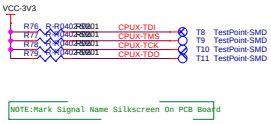
SOC&DDR&PMU mask clamp



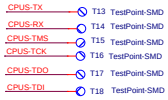
CPUX DEBUG



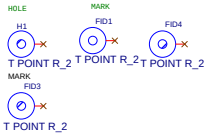




CPUS DEBUG



ASSEMBLE



FEL

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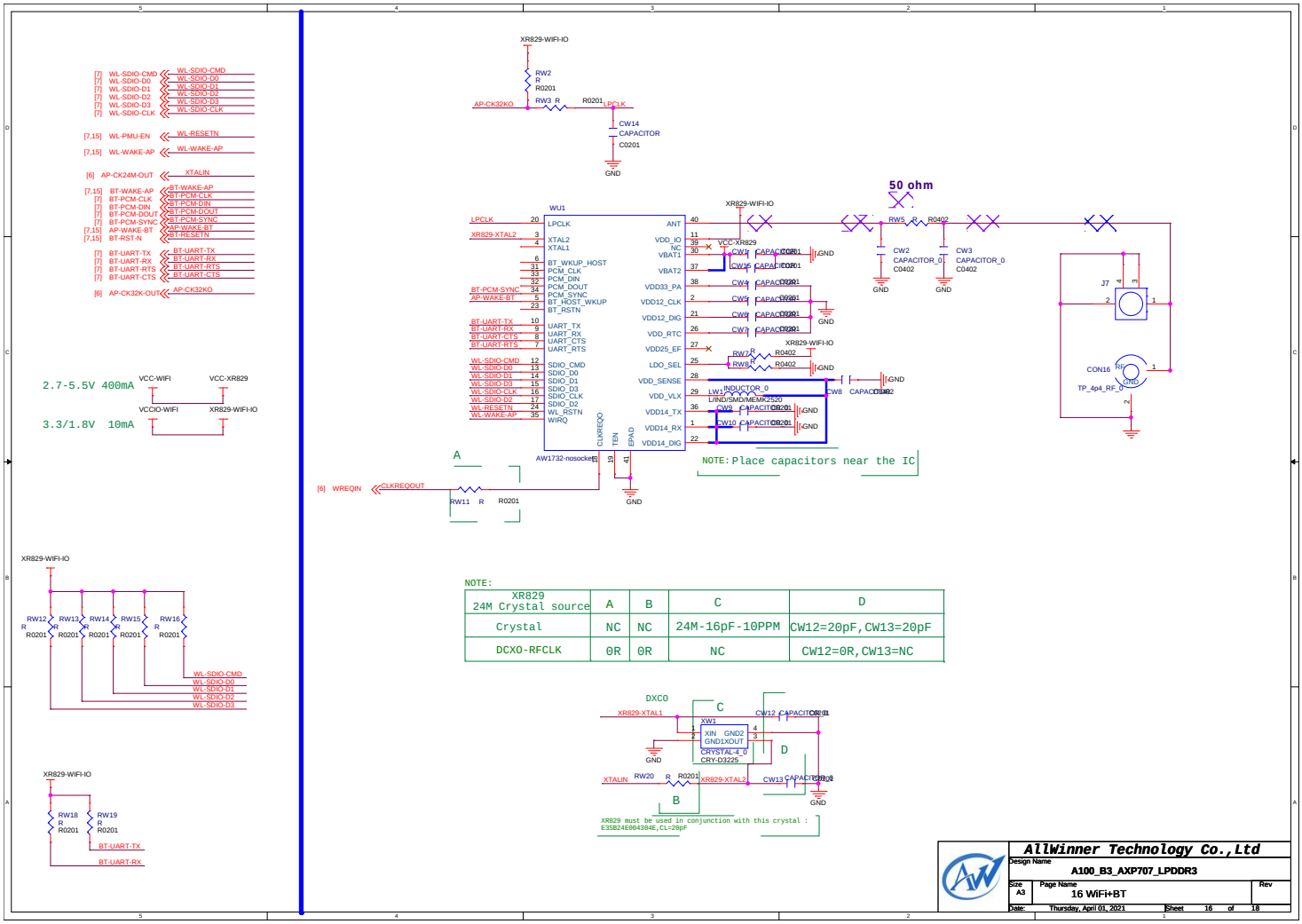
WL-SDIO-CMD
WL-SDIO-D0
WL-SDIO-D1
WL-SDIO-D2
WL-SDIO-D3
WL-SDIO-CLK
WL-PMU-EN
WL-RESETN
WL-WAKE-AP
AP-CK24M-OUT
XTALIN
BT-WAKE-AP
BT-PCM-CLK
BT-PCM-DIN
BT-PCM-DOUT
BT-PCM-SYNC
AP-WAKE-BT
BT-RST-N
BT-UART-TX
BT-UART-RX
BT-UART-RTS
BT-UART-CTS
AP-CK32K-OUT
2.7-5.5V 400mA
VCC-WIFI
VCC-XR829
VCCIO-WIFI
XR829-WIFI-IO
3.3/1.8V 10mA
XR829-WIFI-IO
RW2 R R0201
AP-CK32KO
RW3 R R0201
LPCLK
CW14 CAPACITOR C0201
GND
WU1
LPCLK
XR829-XTAL2
BT_WKUP_HOST
PCM_CLK
PCM_DIN
PCM_DOUT
PCM_SYNC
BT_HOST_WKUP
BT_RSTN
UART_TX
UART_RX
UART_CTS
UART_RTS
SDIO_CMD
SDIO_D0
SDIO_D1
SDIO_D3
SDIO_CLK
SDIO_D2
WL_RSTN
WIRQ
CLKREQO
TEN
EPAD
AW1732-nosocket
ANT
VDD_IO
NC
VBAT1
VBAT2
VDD33_PA
VDD12_CLK
VDD12_DIG
VDD_RTC
VDD25_EF
LDO_SEL
VDD_SENSE
VDD_VLX
VDD14_TX
VDD14_RX
VDD14_DIG
VCC-XR829
CW1 CAPACITOR C0201
CW15 CAPACITOR C0201
CW4 CAPACITOR C0201
CW5 CAPACITOR C0201
CW6 CAPACITOR C0201
CW7 CAPACITOR C0201
RW7 R R0402
RW8 R R0402
LW1 INDUCTOR_0 L/IND/SMD/MEMR2520
CW9 CAPACITOR C0201
CW10 CAPACITOR C0201
CW8 CAPACITOR C0402
50 ohm
RW5 R R0402
CW2 CAPACITOR_0 C0402
CW3 CAPACITOR_0 C0402
J7
CON16
TP_4p4_RF_0
NOTE: Place capacitors near the IC
A
[6] WREQIN
CLKREQOUT
RW11 R R0201
XR829-WIFI-IO
RW12 R R0201
RW13 R R0201
RW14 R R0201
RW15 R R0201
RW16 R R0201
WL-SDIO-CMD
WL-SDIO-D0
WL-SDIO-D1
WL-SDIO-D2
WL-SDIO-D3
XR829-WIFI-IO
RW18 R R0201
RW19 R R0201
BT-UART-TX
BT-UART-RX
NOTE:
XR829 24M Crystal source | A | B | C | D
Crystal | NC | NC | 24M-16pF-10PPM | CW12=20pF,CW13=20pF
DCXO-RFCLK | 0R | 0R | NC | CW12=0R,CW13=NC
DXCO
C
XR829-XTAL1
XW1
XIN GND2
GND1XOUT
CRYSTAL-4_0
CRY-D3225
CW12 CAPACITOR C0201
D
XTALIN
RW20 R R0201
XR829-XTAL2
CW13 CAPACITOR C0201
B
XR829 must be used in conjunction with this crystal : E3SB24EB04384E,CL=20pF
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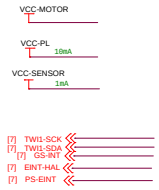
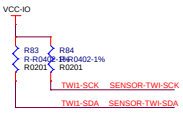
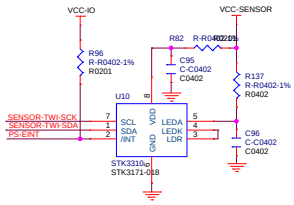


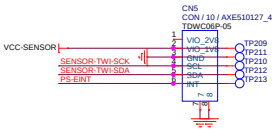


ALS Sensor

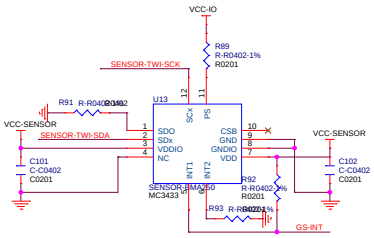


I2C Address: 0x48

ALS Sensor CON

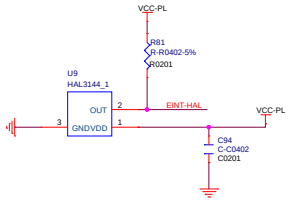


3axis G-sensor

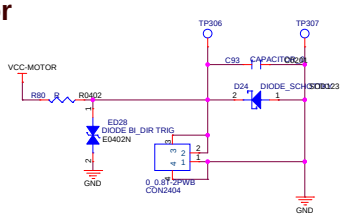


I2C Address: 0x19

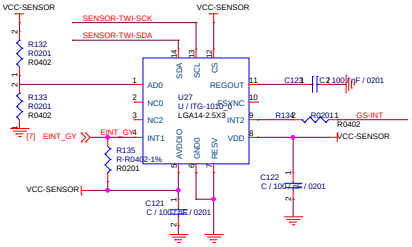
Hall switch



Motor



Gyro Sensor



AllWinner Technology Co.,Ltd		
Design Name: A100_B3_AXP803_LPDDR3		
Size: A3	Page Name: 17 SENSOR	Rev
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